Electronic Version
Stylesheet Version v1.1.1

Method and System For A Variable Frequency SDRAM Controller

Abstract

A method for providing a variable frequency clock for a SDRAM. First, receiving a clock with a fixed frequency and a plurality of signals, wherein each the signal is an interlace combination of a plurality of high level signals and a plurality of low levels signals. Second, extracting a plurality of proper positions from the signals, wherein each low level of each the signal corresponds to a proper position. Third, amending the frequency of the clock such that each the proper position corresponds to a rising edge of the clock.